Low-Noise, High-Precision Bioamplifier with Integrated Delta-Sigma ADC in 130nm CMOS for ExG Signal Acquisition in Human-Machine Interface Applications

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***Abstract*—This paper presents the design and simulation of a low-noise, high-precision bioamplifier system with an integrated Delta-Sigma ADC for ExG signal acquisition, implemented using the Skywater 130nm PDK in Cadence Virtuoso. The system is designed for human-machine interface applications requiring high-fidelity biopotential signal recording. The integrated bioamplifier has a theoretical gain of about 84 dB. The complete system includes a low-noise frontend amplifier, a Delta-Sigma ADC, and supporting circuitry. Simulation results demonstrate an average power consumption of 66.5 µW making it suitable for human-machine interface and wearable applications. The design is verified through comprehensive component-level and full-system simulations in Cadence Virtuoso.**

***Index Terms*—Bioamplifier, Delta-Sigma ADC, ExG Signal Acquisition, Human-Machine Interface, Neural Recording, Low-noise Design**

I. Introduction

The advancement of human-machine interfaces and wearable healthcare devices has driven increasing demand for high-precision bioelectrical signal acquisition systems [1], [2]. These systems must effectively record various electrophysiological (ExG) signals, including electroencephalogram (EEG), electrocardiogram (ECG), and electrogastrogram (EGG), which span a wide range of amplitudes and frequencies. Recent neural recording experiments show that extracellular spikes range from several µV to several hundreds of µV, while local field potentials (LFPs) and power line interferences can reach the mV range [1].

A significant challenge in ExG signal acquisition is the simultaneous handling of these diverse signal characteristics while maintaining high precision and low noise performance. The bandwidth requirements are particularly demanding, as EGG signals can be as low as 0.033 Hz while neural spikes can extend beyond 1kHz [1]. Moreover, electrode-tissue interface offsets and motion artifacts can easily saturate conventional recording systems, limiting their effectiveness in practical human-machine interface applications [2].

Traditional neural recording architectures face several fundamental limitations:

1) Limited dynamic range preventing simultaneous recording of µV-level neural signals and mV-level artifacts
2) Insufficient bandwidth for capturing both ultra-slow biopotentials and fast neural dynamics
3) Poor recovery time from system saturation due to motion artifacts
4) High power consumption limiting practicality for long-term wearable applications

To address these challenges, this paper presents a novel biopotential amplifier with an integrated Delta-Sigma ADC, designed and simulated using the Skywater 130nm PDK in Cadence Virtuoso.

The remainder of this paper is organized as follows: Section II describes the circuit design in the Skywater PDK. Section III presents simulation results and performance characterization. Section IV is a discussion of future work, while Section V concludes the paper.

II. Circuit Design

The circuit design is a one-channel analog-to-digital converter where the differential biopotential signal is capacitively coupled to the OTA through the input capacitor C_{in} (2.2 pF). Consequently, the input signal is integrated by the following integrator. The outputs of the integrator are digitized by a comparator. The noisy comparator output is passed to SR Latch, which further feedback through a digital-to-analog converter to the ADC input stage.

A. Cascode Differential OTA with CMFB

The main amplifier of this circuit is designed using Operational Transconductance Amplifier (OTA). To reduce the input-referred noise while optimizing power consumption, the OTA is implemented as a fully differential, current-reuse architecture. As shown in Fig. 2, cascode OTA is used to achieve high voltage gain and higher bandwidth. The voltage

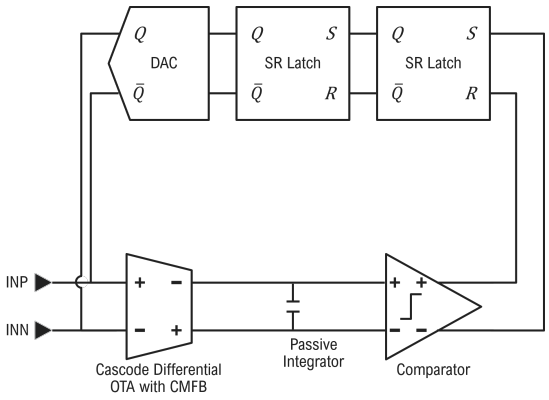

Fig. 1. System-level block diagram of the bioamplifier showing signal flow through OTA, passive integrator, comparator, SR latch, and DAC stages.

gain of the OTA is dependent on bias current (I_{bias}) and W/L of the MOSFETs, by changing these parameters we can achieve the desired gain. The circuit designed is implemented in [1].

A common-mode feedback circuit (CMFB) is designed to stabilize the fully-differential OTA as shown in Fig. 3. This circuit compares the outputs of the OTA to common-mode voltage (V_{CM}) to generate an output voltage controlling the bias current entering the OTA which balances the common-mode.

Here, V_{DD} is 1.2 V and GND is 0 V, so V_{CM} is 0.6 V. With I_{bias} of 100 µA we are able to achieve voltage gain of 150.

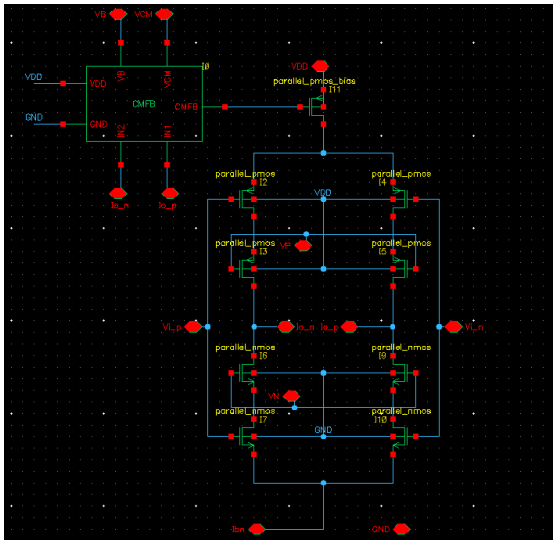

Fig. 2. Schematic of the folded-cascode OTA with integrated CMFB circuitry

B. Passive Integrator

For lowering the power consumption a passive integrator which consists of a capacitor C_{int} (100 pF) is used to integrate the differential output of the OTA.

C. StrongARM Comparator

A comparator was used to digitize the output of the OTA and transmit feedback to the DAC/SR latch. A StrongARM

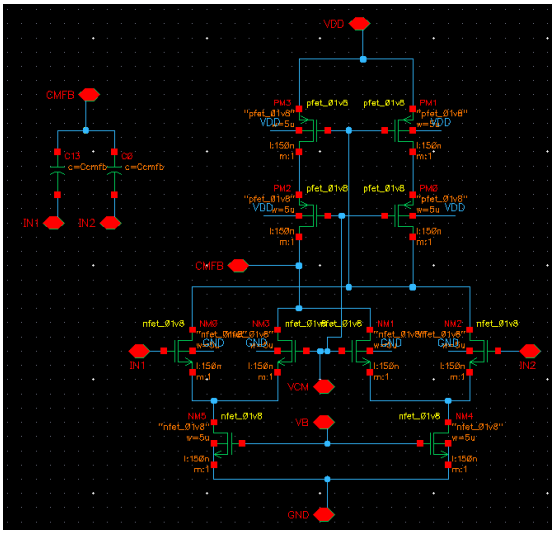

Fig. 3. Schematic of common-mode feedback circuit

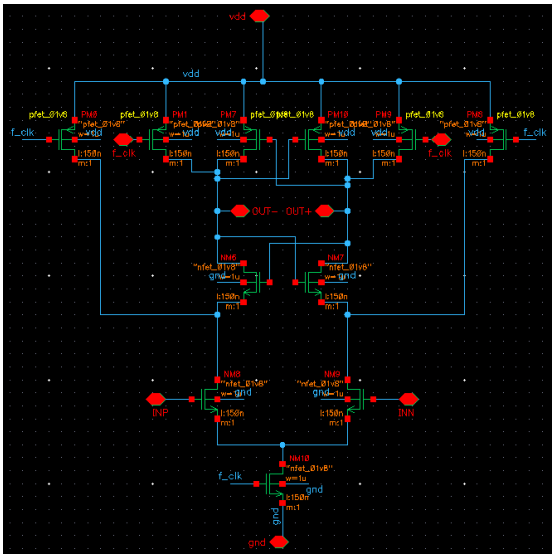

Fig. 4. StrongARM comparator schematic showing differential pair and cross-coupled stages

latch topology allows elimination of static power, provides rail-to-rail output, and reduces input-referred offset [4]. The latch consists of a clocked differential pair, two cross-coupled pairs, and four precharge switches. Binary output is provided in response to the polarity of V_{INP}-V_{INN}. For a positive difference (V_{INP} greater), 1 (VDD) is outputted; for a negative difference (V_{INN} larger), 0 is outputted. The clocked quadratic pulse (f=100 kHz) generates an output value every 10 µs and achieves higher accuracy and lower power compared to a continuous comparator. These latched/dynamic comparators employ strong positive feedback for a ”regeneration phase” when clock is high, and have a ”reset phase” when clock is low.

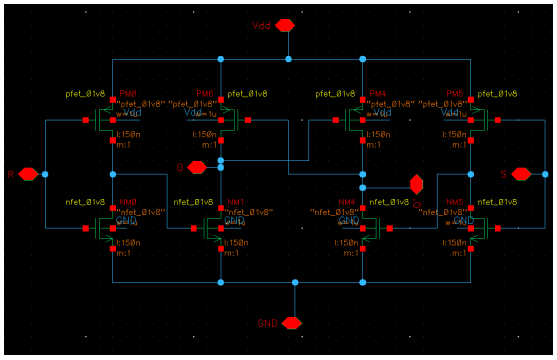

Fig. 5. SR latch implementation using cross-coupled NAND gates.

D. SR Latch

The SR (Set-Reset) Latch is implemented using W/L (1u/150nm) NMOS and PMOS transistors configured as two NAND gates. When S is high and R is low, the output becomes high, and when R is high and S is low, the output Q becomes low [5]. The latch holds the comparator output, providing stable high or low voltage outputs. Due to observed oscillations around the 0 bit, two SR latches were implemented in series for improved stability.

E. DAC

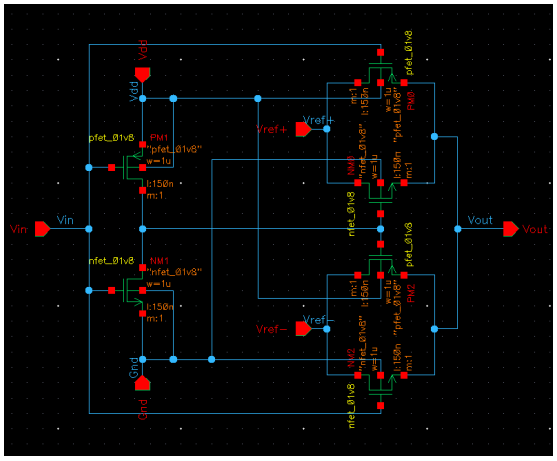

Fig. 6. 1-bit DAC implementation using transmission gates.

A 1-bit digital-to-analog converter (DAC) converts the digital SR Latch output into an analog signal for feedback to the ADC input stage. Depending on the digital input (1 or 0), the DAC outputs either V_{ref+} or V_{ref-}, ensuring compatibility between the feedback and analog input signals. This logic is implemented using a 2×1 multiplexer with transmission gates controlled by the SR Latch output and its inversion [6]. The design operates efficiently in a 130 nm CMOS process using two reference voltages and achieves reliable signal conversion for delta-sigma modulation.

III. Simulation Results

A. Differential OTA with CMFB

For the circuit, the W/L values for the OTA's pmos transistors are 300u/280n and the nmos transistors are 440µ/270n. The CMFB circuit's all MOSFETs have W/L of 5u/150n. Other parameters are as follows: V_{DD} = 1.2 V, V_{CM} = 0.6 V, I_{bias} = 100 µA. As shown in Fig. 8 for an input of 1 µV 200 Hz sine wave we observe gain of 43.53 dB.

B. Comparator and SR Latch Simulation

The Strong ARM comparator and SR Latch designs were implemented in 1 µm and 150 nm CMOS process using Cadence Virtuoso. The schematic diagram of both components is shown in Fig. 4 and Fig. 5. For testing, we used:

- Sinusoidal input: f_{sine} = 200 Hz, V_{sine} = 0.1 mV
- Clock frequency: f_{clk} = 100 kHz
- Supply voltage: VDD = 1.2 V
- Common mode voltage: V_{CM} = 0.6 V
- Differential inputs: V_{INN} = V_{CM} + 0.1 mV, V_{INP} = V_{CM} - 0.1 mV

We completed a transient analysis over 10 ms. The response is shown in Fig. 9 and displays the dynamics anticipated with V_{OUTP} and V_{OUTN} following the clock and jumping between 0 and V_{DD}.

C. Full System Simulation

Fig. 7 shows the entire circuit consisting of all the components discussed above put together. Here, the input signal V_{i_p} & V_{i_n}, integrator output V_{int_p} & V_{int_n}, comparator output V_{comp_p} & V_{comp_n}, output signal (SR Latch output) V_{out_p} & V_{out_n} and DAC feedback V_{DAC_p} & V_{DAC_n}.

We can see that for an input signal of 200 Hz 0.5 mV, we get the desired output as shown in Fig. 10. Comparator outputs are not included in the plot. Fig. 11 shows the set of design parameters.

IV. Discussion and Future Work

A. Circuit Performance

As seen in Fig. 10, V_{out_p} & V_{out_n} show the desired output, the output signal changes with varying differences in the input signal. However, the implemented bioamplifier system gives the desired output only for input voltage above 0.5 mV. In addition, the average power consumption of the entire circuit is 66.5 µW.

B. Future Directions

Future work will focus on enhancing the bioamplifier's performance and versatility in several key areas:

1) Enhanced Sensitivity: Design optimization for nV-range input signals to detect weaker biopotentials, enabling broader application in neural recording and fine-grained biosignal detection.

2) Power Optimization: Further reduction in power consumption to support long-term wearable or implantable applications, with particular focus on dynamic power scaling and improved circuit topology efficiency.

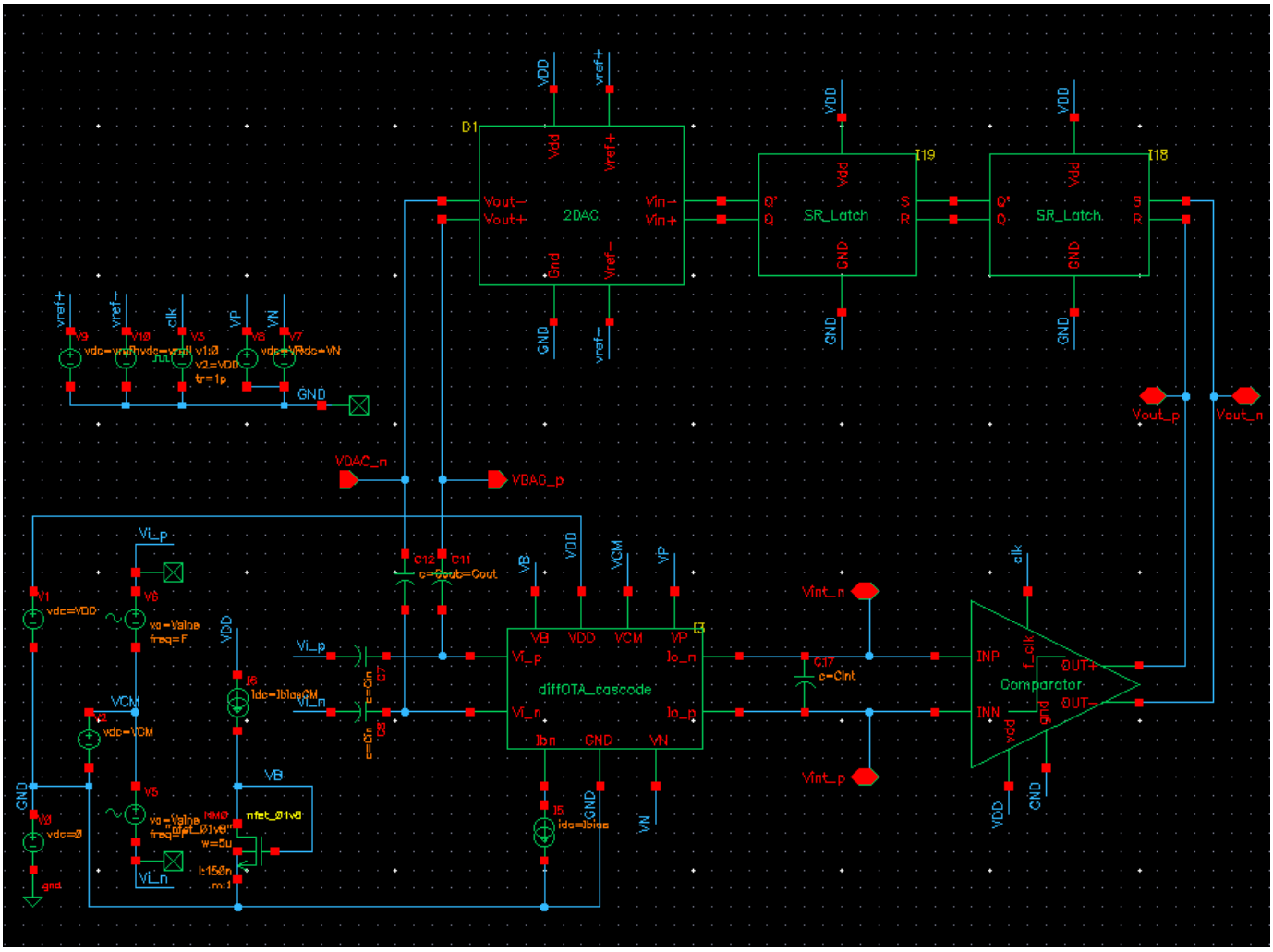

Fig. 7. Full circuit schematic

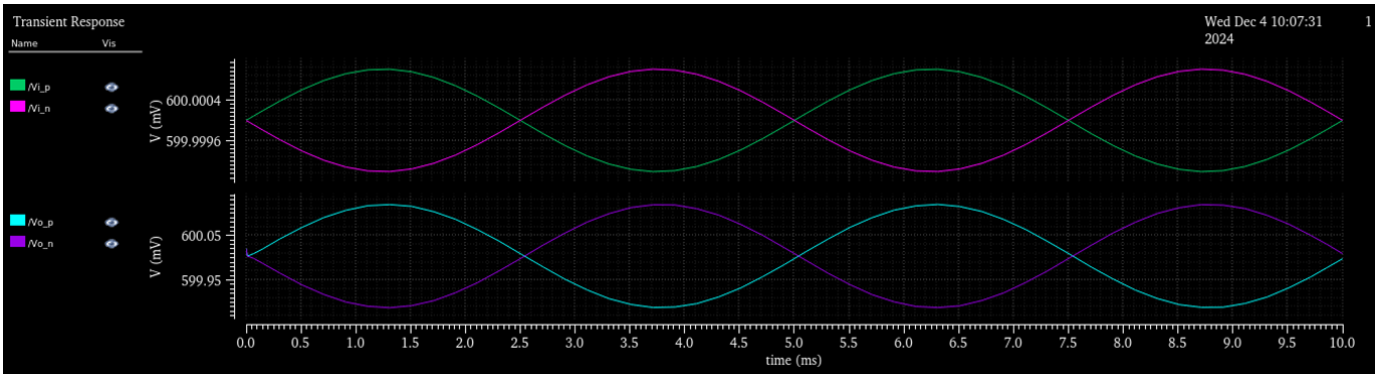

Fig. 8. Transient analysis of OTA with CMFB

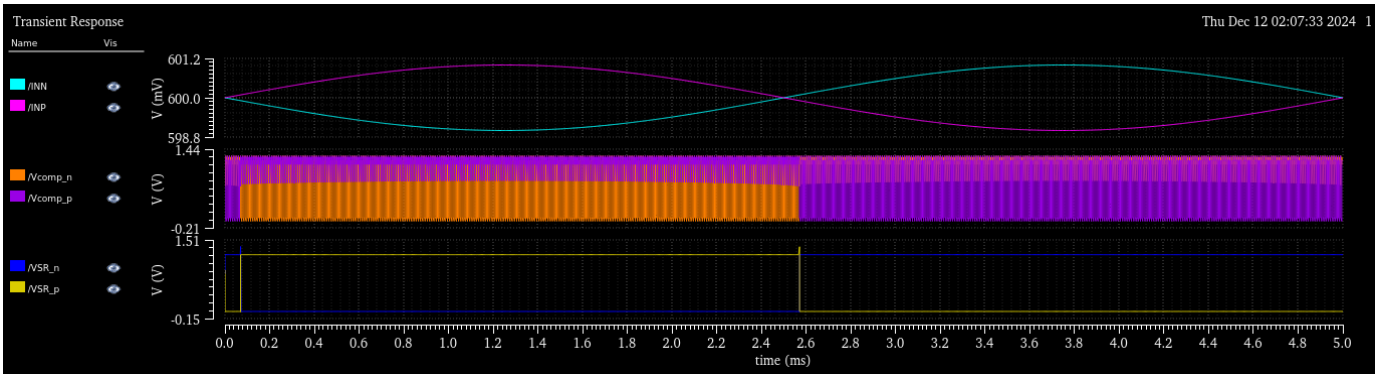

Fig. 9. Transient analysis of comparator and SRLatch

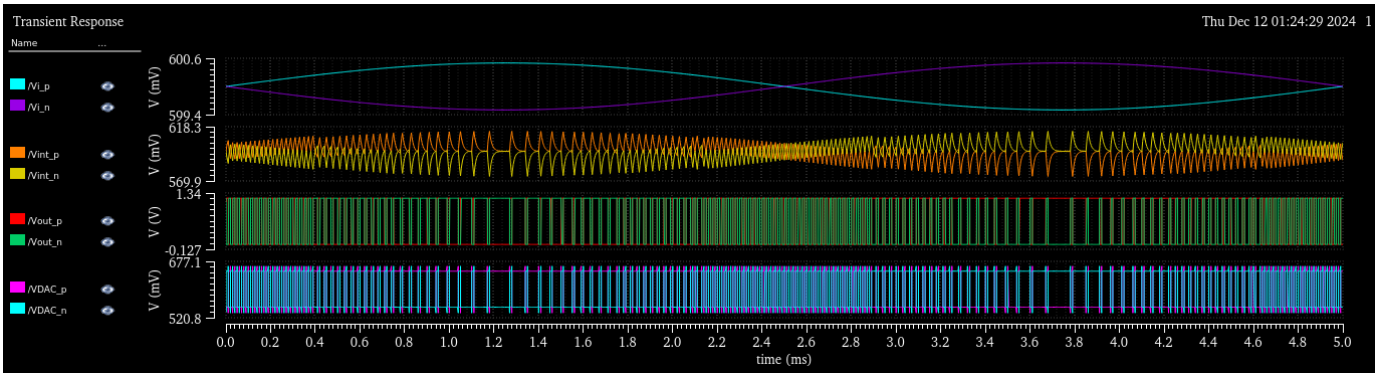

Fig. 10. Transient analysis of complete system

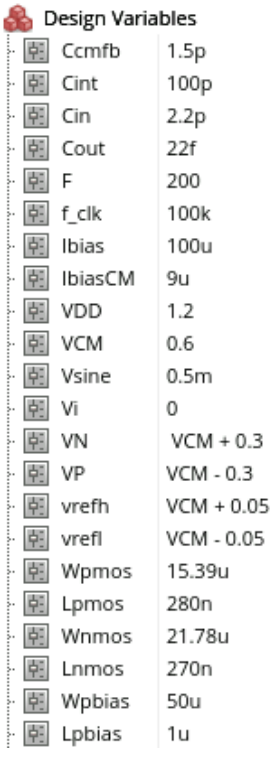

Fig. 11. Design parameters of full circuit

3) Signal Fidelity Improvements: Refinement of noise suppression and filtering techniques through advanced filtering algorithms and improved common-mode rejection.

4) Multi-Channel Development: Expansion into a multi-channel system enabling simultaneous recordings from multiple electrodes for comprehensive physiological monitoring.

V. Conclusion

This work presents a comprehensive implementation of a low-noise bioamplifier system with integrated delta-sigma ADC in 130nm CMOS technology. Through careful optimization of each component - from the front-end OTA to the feedback DAC - the system demonstrates robust performance in ExG signal acquisition. The implemented architecture provides a foundation for future developments in multi-channel biosignal acquisition systems, with particular promise for human-machine interface applications.

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